**North South University**

Department of Computer Science and Engineering

**Final,** Fall-2016

Course No: **CSE231** Course Title: **Digital Logic Design**

Time:1 h 30 min Full Marks: 40

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| 1. | The full adder receives two external inputs x and y, the third input Q comes from the output of a D-flip-flop. The carry output is transferred to flip-flop very clock pulse. The external output S gives the sum of x, y, and Q. Obtain the state table and the state diagram of the sequential circuit. | 7 |
| 2. | Design a sequential circuit that can detect 3 or more consecutive 1’s using D flip-flop | 10 |
| 3. | Design a 8x4 ROM with the following contents.   |  |  | | --- | --- | | Address | Data | | 000 | 0001 | | 001 | 0010 | | 010 | 0100 | | 011 | 0000 | | 100 | 0011 | | 101 | 0110 | | 110 | 0111 | | 111 | 0101 | | 5 |
| 4. | This is an extension of Q3. Here, you have to design a circuit that can read a content of ROM ( as designed in Q3 ) and multiply it with 2. The block diagram is provided. You can consider using the circuit you designed in question 3.  Read ROM data and multiply by x 2  Sample output *0100*  Sample Input *001* | 8 |
| 5. | Reduce the number of state in the following state table, tabulate the reduced table, and draw the state diagram   |  |  |  |  |  | | --- | --- | --- | --- | --- | | **Present State** | **Next State** | | **Output** | | | **x = 0** | **x = 1** | **x = 0** | **x = 1** | | *a* | *f* | *b* | 0 | 0 | | *b* | *d* | *c* | 0 | 0 | | *c* | *f* | *e* | 0 | 0 | | *d* | *g* | *a* | 1 | 0 | | *e* | *d* | *c* | 0 | 0 | | *f* | *f* | *b* | 1 | 1 | | *g* | *g* | *h* | 0 | 1 | | *h* | *g* | *a* | 1 | 0 | | 10 |
| 6. | (Bonus) Transfer following statement into logical circuit :  If (x = = y)  A = x  Assume that, x and y are 2 bit data and A is a 2 bit register. | 5 |